09:00-09:10: Welcome Speech, Francesco Brancati, Resiltech s.r.l.

09:10-10:00 Keynote – Towards Effort and Quality Estimation of V&V Processes. – Andras Pataricza, Department of Measurement and Information Systems, Budapest University of Technology and Economics.

10:00-11:00 Session 1: Model checking approaches:
Session Chair: Barbara Gallina, Mälardalen University.

• “Verification of fault-tolerant system architectures using model checking”
  Jussi Lahtinen;

• “Verification of a real-time safety-critical protocol using a modelling language with formal data and behaviour semantics”
  András Vörös, Tamás Tóth and István Majzik;

11:00-11:30: Coffee Break

11:30-12:30 Session 2: Tools:
Session Chair: Ilaria Matteucci, IIT-CNR.

• “Visualization of Model-Implemented Fault Injection Experiments”
  S. Daniel Skarin, Jonny Vinter and Rickard Svenningsson;

• “Cost-Effective Testing for Critical Off-The-Shelf Services”
  Fabio Duchi, Nuno Antunes, Andrea Ceccarelli, Giuseppe Vella, Francesco Rossi and Andrea Bondavalli.

12:30-13:00 Session 1&2 Closing Discussion

13:00-14:30 Lunch

14:30-15:30 Session 3 System and tool assessment:
Session Chair: Nuno Antunes, University of Coimbra.

• “On Security Countermeasures Ranking through Threat Analysis”
  Andrea Bondavalli, Andrea Ceccarelli, Felicita Di Giandomenico, Fabio Martinelli, Ilaria Matteucci and Nicola Nostro;

• “Enabling Cross-domain Reuse of Tool Qualification Certification Artefacts”
  Barbara Gallina, Shaghayegh Kashiyarandi, Karlheinz Zugsbratl and Arjan Geven;

15:30-16:00 Session 3 Closing Discussion

16:00-16:30: Coffee Break

16:30-17:20 Panel Discussion: “Towards cost-effective certification of critical systems: is it really possible?”
Panelists:

• Philip Koopman, Carnegie Mellon University
• Henrique Madeira - University of Coimbra
• Vincenzo Manni – RINA Services

17:20-17:30 Conclusions & Closing Remarks, Francesco Brancati, Resiltech s.r.l.

For more details, contact the organizing committee or visit:
http://www.cecris-project.eu/DEVVARTS
This workshop is organized within the FP7 PEOPLE-IAPP project CECRIS.
http://www.cecris-project.eu/
Keynote Talk Title:
Towards Effort and Quality Estimation of V&V Processes.

Speaker
Andras Pataricza
Department of Measurement and Information Systems
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Abstract:
Cost estimation was developed based on the experiences of large SW industries. Development processes in such enterprises are typically performed entirely in-house and rely on a monolithic design, implementation and test culture. Accordingly, most cost estimators look at the development process at large. Even the model of finest granularity takes for instance testing as a single elementary activity.

However; V&V of critical applications becomes more and more to a core activity of specialized SMEs performing only specific parts of the checking process. Unfortunately, no KPI estimator exists at the resolution of individual steps (requirement V&V, test specification, test implementation etc.) for checking critical systems. The lack of fine granular cost estimators focusing on the individual activities related to V&VA and certification becomes to a critical bottleneck for instance in the embedded systems (ES) industry. Depending on the level of criticality and complexity, the share of V&V in the total effort of an ES design is the same or one order of magnitude higher compared to that related to functional design and implementation. Technology development for instance introduction of sophisticated formal methods for V&V necessarily involves upgrade of the skills of the personnel. The total cost related to the introduction a new technology needs a calculation of RoI (return of investment), especially in SMEs specialized to V&V.

Creating V&V specific cost estimators is a promising task by following same approach as it was done for overall software development. V&V and certification related sub-processes are just another specific kind of software processes. For instance, implementation testing may start from the very same specification as functional design and has to deliver test programs (testing based validation) or a executable abstract system model described in some automata theory oriented programming language (formal validation).

Prof. Andras Pataricza.

András Pataricza graduated in Electrical Engineering, holds a DsC. degree from the Hungarian Academy of Sciences, and a Dr-habil. from BUTE. In 1994 he founded the Fault-Tolerant Systems Research Group at the Department of Measurement and Information Systems. He served as visiting professor at the University of Erlangen and at the CASED in Darmstadt. He received multiple recognition awards from different scientific and industrial organizations. He served as the Steering Committee Chair of the Hungarian ARTEMIS National Technology Platform. In 2006 he was a founding member as visiting professor of the IBM Budapest CAS (Center of Advanced Studies). He has acted as technical leader and/or advisor to many international scientific projects and EU scientific research programs. He has published over 130 papers in international journals, conferences and workshops in the field of Dependable Computing, Embedded System and Model-Driven Engineering. He served among others as the General Chair of the Annual 43th IEEE/IFIP International Conference on Dependable Systems and Networks (DSN 2013). In 2014 he was elected to be a member of IFIP WG10.4. on Dependable Computing and Fault Tolerance.

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